

MOHAMMED ABDUL HAQ

abdulhaq7123@gmail.com — +91-9381230889

[LinkedIn Profile](#)

Summary:

An M.Tech student specializing in RTL design and verification with a strong passion for digital electronics, VLSI design, and cutting-edge semiconductor technologies. Proficient in Verilog, SystemVerilog, UVM, and Python, with hands-on experience in FPGA and ASIC design projects. Demonstrates a strong commitment to delivering high-quality, innovative solutions and expertise in project management, digital design, and prototype development.

Experience:

RTL Design Engineer — WiSig Networks @ IIT Hyderabad

July 2024-Present

- Designed and implemented Verilog HDL on FPGAs, achieving a 20% reduction in processing latency for digital signal applications.
- Authored detailed technical documentation using LaTeX, enhancing cross-team collaboration and reducing project misalignment by 15%.
- Contributed to developing digital hardware solutions for 5G and 6G networks, demonstrating expertise and innovation.

Design and Verification Engineer — Tech Mahindra Cerium Systems *August 2022-July 2023*

- Led the development of dynamic simulation verification procedures utilizing Verilog, SystemVerilog, UVM, and Synopsys EDA tools (VCS, Verdi).
- Standardized UVM testbench architecture templates for strong test coverage of ASIC and SOC designs.
- Reduced debugging time by 50% by balancing duties, managing client relationships, and providing frequent project updates.

Projects:

AXI Stream-Based PDCCH for 5G Application

September 2024-November 2024

- Built a top-level module with a synchronous FIFO and configurable router for a 32-bit datapath using AXI standards.
- Reduced utilization by 30

PN-Sequence Generator for Real-Time 5G Applications

July 2024-August 2024

- Developed and deployed a PN Sequence Generator with one-hot encoding, validated in MATLAB, achieving a 25% Utilization optimization on FPGA.
- Simulated the AXI-based generator with MATLAB-generated inputs and outputs for precise functionality verification.

Test Bench for Ethernet Switch Protocol IEEE 802.3-2018

May 2023-July 2023

- Generated a UVM Test Bench to accommodate the Ethernet switch.

- Regression tests and debugging were performed, achieving 96% coverage.

Design and Verification of Communication Protocols

December 2022-December 2023

- Produce and verify communication protocols, including FIFO (Sync/Async), AHB, APB, AXI, I2C, SPI and UART.
- Streamlined implementation and validation for efficiency and reliability.

RISC-V Implementation using Open-Source EDA Tools

November 2021-February 2022

- Developed RTL code for the pipeline module of the RISC-V.
- Used Open Lane and Q-flow for back-end design ASIC processes.

Education:

University of Hyderabad

2023-2025

M.Tech in Microelectronics and VLSI Design

CGPA: 8.93

MJCET

2018-2022

B.E. in Electronics and Communication

CGPA: 7.99

Skills:

Programming Languages: Verilog, SystemVerilog, C/C++, Python

Core Subjects: Digital Electronics, UVM, STA, CMOS Concepts, SVA, CDC, Linting

Tools: Xilinx Vivado, Intel Quartus Prime, Modelsim, Synopsys VCS, Verdi, Cadence Toolkit (Virtuoso, Innovus, Genus), MATLAB, Jira

Protocols: I2C, SPI, UART, APB, AHB, AXI, Ethernet

Certifications:

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- Certification of "Verilog, SystemVerilog, UNIX, and UVM" from Cerium Systems *September 2022-November 2022.*
 - Certification of "Verilog HDL Programming Python Programming" from UDEMY *August 2022-October 2022.*

Co-Curricular Activities:

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- Organized RISC-V Road Show program.
 - Organized an IEEE event involving 50+ participants.